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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,912	08/26/2003	Heemyoung Park	FIS920030026US1	1911

29154 7590 05/03/2005

FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,912	PARK ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on June 24, 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2-4, 10, 11 and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Although an attempt has been made to identify all instances of claim language non- complacence, such identification is extremely burdensome due to the large number of instances. Examples are provided herein below. Since such noncompliance confuses the claims to the extent that not all of the problems are ready apparent, then upon amendment, if an alternative interpretation of claim language requires a change in the rejection, the new rejection may properly made final.

Claims 2 and 17 recite the limitation "wherein the height of said gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by said spacers" in lines 1-4.

However the recited limitation is not clear in its meaning and scope for the following reasons:

What does it mean by "the height of said gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by said spacers?"

Does it mean that the gate has two different height?

Which height of the gate is associated with spacing of the source and drains?

Does it mean the width of the gate electrode? And etc.

Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3, 10 and 18 recite the limitation "wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer, such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone" in lines 1-5.

However, the recited claim lacks clarity in its meaning and scope for the following reasons:

What does mean by "wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer?"

How the size of the spacer can be controlled by the combined height of said gate conductor and said sacrificial layer? Is that in terms its thickness? Is that in terms its height? Is that in terms of its width? And ect.

Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, 11 and 19 also rejected as being dependent of the rejected base claim.

Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

In light of the rejection 35 U.S.C. § 112 second Paragraph *supra*, the following 35 U.S.C. 102 rejection for claims 2-4, 10, 11 and 17-19 is based on prior art which reads on the interpretation the claim language of the instant application as best as understood by the Examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1- 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (US/6,429,084).

Re claim 1, park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate (i.e., SOI substrate), a gate conductor (50) above the substrate (see Fig. 1), and at least one sacrificial layer (51 52 54) above the gate conductor (50); patterning the laminated structure into at least one gate stack (55) extending from the substrate (see Fig. 1) (Col. 1, lines 50-65) ; forming spacers (60 70) adjacent said gate stack (55) (see Fig. 2); doping regions of the substrate not protected by the spacers (60 70) to form source and drain regions adjacent the gate stack (55); and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 2, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein the height of the gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by

said spacers (i.e., the distance of space between the source and drain is larger that of the height of the gate conductor) (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 3, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer, such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 4, as applied to claim 3 above, Park et al. disclose all the claimed limitations including the limitation wherein said larger spacing positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 5, The method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 6, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 7, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises doping source/ drain electrodes and said gate conductor together in a self-aligned implantation after said

patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 8, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises a first doping process of doping source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 9, Park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, themethod comprising: forming a laminated structure having a substrate (see Fig. 1), a gate conductor (50) above the substrate, and at least one sacrificial layer above said gate conductor (see Fig. 1); patterning said laminated structure into at least one gat stack extending from said substrate; forming spacers adjacent said gate stack; epitaxially growing raised source and drain regions on said substrate adjacent said gate stack (see Fig. 5); implanting impurities into said raised

source and drain regions and into said substrate; and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 10, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer, such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 11, as applied to claim 10 above, Park et al. disclose all the claimed limitations including the limitation wherein said larger spacing positions said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 12, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer, wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 13, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises doping said source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas,

without said sacrificial layer, said doping process would implant an impurity through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 14, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises a first doping process of doping source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 15, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein by implanting said impurities after said epitaxially growing process, said impurities avoid being subjected to the thermal budget of said epitaxially growing process (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 16, Park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor; patterning said laminated structure into at

least one gate stack extending from said substrate; epitaxially growing raised source and drain regions on said substrate adjacent said gate stack, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities; implanting impurities into said raised source and drain regions and into said substrate, removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 17, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein the height of said gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by said spacers (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 18, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer, such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 19, as applied to claim 18 above, Park et al. disclose all the claimed limitations including the limitation wherein said larger spacing positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 20, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said

gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 21, as applied to claim 20 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 22, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises doping said source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 23, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises a first doping process of doping source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant

impurities through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 24, Park et al. disclose a method of producing an integrated circuit transistor comprising: forming a laminated stack deposition, wherein said laminated stack deposition is formed in a process comprising: forming a silicon layer over a substrate layer (30) (i.e., part of SOI); forming a gate oxide (40) on said silicon layer (30); forming a gate conductor (50) on said gate oxide (40); and forming of least one sacrificial material above said gate conductor, patterning said gate oxide (see Figs. 5 and 6), gate conductor, and said sacrificial material into at least one gate stack (see Figs. 1-6); forming temporary spacers (70 60) adjacent said gate stack (55); epitaxially growing raised source and drain regions (36) (see Fig. 6) above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack; growing an additional dielectric layer (44) (see Fig. 8) on said raised source and drain regions (36); removing said temporary spacers (see Fig. 9) without removing said sacrificial material (51) ; performing a halo implant (see Fig. 10) in said raised source and drain regions and in exposed regions of said silicon layer; forming a permanent spacer (80) (see Fig. 11) adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer; implanting impurities into said raised source and drain regions and exposed regions of said silicon; forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions; implanting additional impurities into said raised source and drain regions and exposed regions of said silicon; annealing to activate all impurities; etching back said additional dielectric layer on said raised source and drain regions; and saliciding both said gate

conductor and said raised source and drain regions (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 25, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 26, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 27, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 28, as applied to claim 31 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Yu (US/6,372,589) and Park et al. (U.S. 6,828,630) also disclose similar inventive subject matter.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

BK
April 29, 2005